REMARKS

I. INTRODUCTION

In response to the Office Action dated May 12, 2005, claims 1, 3, 4, 9, 17, 18, 20, 25, 32, 33, 35, 37, 41, 42, 45, and 48 have been amended. Claims 1-48 remain in the application. Entry of these amendments, and re-consideration of the application, as amended, is requested.

II. CLAIM AMENDMENTS

Applicants' attorney has made amendments to the claims as indicated above. These amendments were made solely for the purpose of clarifying the language of the claims, and were not required for purposes of patentability.

III. STATUS OF CLAIMS

Claims 1-48 are pending in the application.

Claims 1-5, 9, 10, 14-22, 25, 26, and 29-48 were rejected under 35 U.S.C. §102(b) as being obvious in view of U.S. Patent No. 3,482,085 to Smith, Jr., and these rejections are traversed.

IV. ISSUES PRESENTED FOR REVIEW

Whether claims 1-5, 9, 10, 14-22, 25, 26, and 29-48 are patentable under 35 U.S.C. § 102(b) over U.S. Patent No. 3,482,085, issued to Smith, Jr.

V. GROUPING OF CLAIMS

The rejected claims do not stand or fall together. Each claim is independently patentable. Separate arguments for the patentability of each claim are provided below.

VI. ARGUMENTS

Claims 1-5, 9, 10, 14-22, 25, 26, and 29-48 are rejected under 35 U.S.C. §102(b) as being anticipated over Smith, Jr., U.S. Patent No. 3,482,085.

A. The Smith Reference

U.S. Patent No. 3,482,085, issued December 2, 1969 to Smith discloses a binary full adder-subtractor with bypass control. The bypass control has the effect of suppressing the arithmetic operation of the adder-subtractor and causing one of the arguments to the operation to be produced at the output; however, the borrow or carry signal is still produced as if the operation had not been suppressed. The bypass control might be generated, for example, as when a negative difference would be produced by the suppressed operation. The adder-subtractor has particular application in matrix arithmetic units capable of the more complex arithmetic operations of multiply, divide, root taking, power generation, etc., and is preferably constructed of semiconductor logic circuits.

B. The Subject Invention

The present invention, evidenced by an adder for adding a signal at a first input *(A)* and a second input *(B)* to produce an adder output *(S)* is disclosed. In one embodiment, the adder comprises a bypass input *(bypass)* and a logic circuit, communicatively coupled to the bypass input *(bypass)*, the first input *(A)*, and the second input *(B)*, the logic circuit configured to hold a value of at least one of the first input *(A)* and the second input *(B)* according to the bypass input *(bypass)*. In another embodiment, the present invention is evidenced by an adder for adding a signal at a first input *(A)* and a second input *(B)* to produce an adder output *(S)*, comprising a bypass input (*bypass*); and a logic circuit, communicatively coupled to the bypass input (*bypass*), the first input *(A)*, and the second input *(B)*, the logic circuit configured to generate the adder output *(S)* without computing a new adder output according to the bypass input (*bypass*).

C. Differences Between the Subject Invention and the Cited References

Applicants respectfully submit that the two bypassable adder circuits, ours and Smith's, while seemingly similar at a superficial level, are totally different in purpose, in structure, and in operation.

With respect to purpose: The purpose of the Applicants' invention is to create a circuit *that does not dissipate power* in those situations where a new value arrives at one of its input terminals and it is desired to *not* perform the addition operation for the new set of inputs. A second purpose is to provide, as desired in particular applications, the bypass of one of the adder inputs to the output

whenever the "no add" situation occurs. Smith, on the other hand, expresses the purpose of providing a conditional bypass capability, but one wherein the output of the carry signal is computed and provided at the adder's carry output terminal just as if the complete adder operation had been performed. This is provided in order that the adder-subtractor have particular application in matrix arithmetic units capable of more complex arithmetic operations. The Smith bypass circuit does not avoid the toggling of logic gates within the adder in those situations wherein a bypass is occurring, as the Applicants' invention does. In fact, by including the additional elements necessary to achieve it's purpose, Smith may well *increase* the power consumption over a standard adder.

Smith does not actually teach "suppressing the arithmetic operations of the adder" as the First Office Action suggests on the bottom line of its page 2, but rather, teaches "...*the effect* [emphasis added] of suppressing the arithmetic operation ..." (see the Smith Abstract). This is an important distinction, as Smith does not, in fact, *suppress* the adder's operation but rather, simply modifies its operation so that, logically, it behaves *as if* the summation operation were bypassed. Even in the bypass mode of operation, Smith's adder still burns power because of the computation it performs to *generate* the "bypass output."

There is a second reason why Smith's adder burns power while in bypass mode - Smith's adder is generating the *carry* output even in those situations where it is computing a bypass output rather than computing the correct sum. In contrast, the Applicants' adder *always* avoids computing (burning power) when in bypass mode.

D. Claims 1, 18, 33, 37, and 45 are Patentable Over the Smith Reference

With Respect to Claim 1: Claim 1 recites:

An adder for adding a signal at a first input (A) and a second input (B) to produce an adder output (S), comprising:

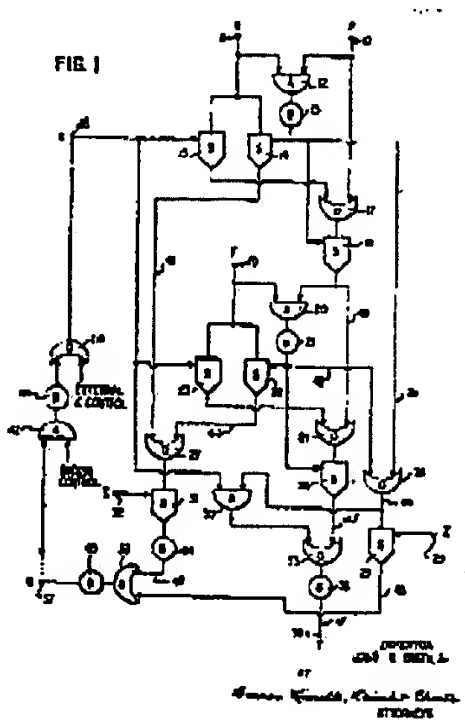
a bypass input (bypass); and

a logic circuit, communicatively coupled to the bypass input (bypass), the first input (A), and the second input (B), the logic circuit configured to hold at least one of a value of the first input (A) and a value of the second input (B) according to the bypass input (bypass).

The First Office Action argued that:

Smith Jr. discloses in figure 1 an adder for adding a first input (E), a second input (P), and a carry input (F) to produce an adder output (T) and a carry out (G). The adder also has a bypass input (K) for controlling the logic of the adder to hold the first input (at 15), the second input (at 18) and the carry input (at 23), and to generate an adder output and carry without computing as claimed (suppressing the arithmetic operations of the adder, see abstract and col. 5, lines 40-71). The element (S, see figure 2d) can be seen as a transmission gate or latch with (a) as a logical input, (b) as clock input, and (c) as an output.

FIG. 1 is reproduced below:



The Applicants respectfully disagreed, pointing out that the Smith reference does not disclose *a logic circuit that holds at least one of the first input and the second input according to the bypass input*, as recited in claim 1. Instead, Smith teaches a system that modifies the operation of the adder so that it produces a modified output, one that is logically the same as if the addition operation were not accomplished. Smith does not "hold" either the first or the second input; rather, it modifies the logic to use the first and second input so that the result of its computation appears as if the operation had been bypassed.

The Final Office Action replied:

> "the recitation 'hold' when broadly interpreted in light of the specification is to stop or prevent a signal from transmitting through something. Therefore, the preventing the first input E from transmitting through element 15, the suppressing the second input P to zero by element 17 to prevent it from passing through element 18, and the preventing the carry F from transmitting through element 23 in adder logic circuit of figure 1 of Smith according to the bypass signal K is clearly read on the invention." (Final Office Action, page 3)

Applicants must disagree. The foregoing interpretation of the term "hold" is not correct when interpreted in light of the specification. Nonetheless, in the interest of clarifying the claims, Applicants have amended the certain claims to further clarify that the inputs to the adder are *held* at their *value*.

It cannot be disputed that the "suppressors" of the Smith reference do not "hold" input values. The truth table for the "suppressor" is shown below:

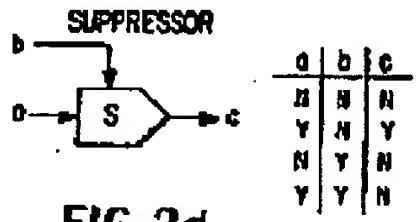


FIG. 2d

Plainly, the suppressor does not hold the input value at "a". As the suppressor circuit has no memory (contrary to the First Office Action's assertion that the foregoing is analogous to a latch), there indeed can be no notion of holding a value as expressed in Applicants' claims. Instead, the suppressor has no effect when the logical input at "b" is N, and forces the logical output "c" to "N" when "b" is Y. When the "bypass" signal "b" is applied, the suppressor of FIG. 2d in fact *changes* the logical value of its output "c". It does not "hold" the input value "a" in any sense of the word. In effect, setting the bypass value "b" to "Y" causes the suppressor's output to always be "N" which will be the correct result half of the time and the incorrect result the other half of the time.

Further, viewed from the perspective of Smith's bypassable adder as a whole, the "holding" aspect of the adder described in Claim 1 is not present. When the bypass is ON, Smith's circuit passes whatever value is at the P input to the output T. If, over time, P varies (while Smith's bypass

remains ON), the T output will vary as well, tracking P's behavior. This is fundamentally different than the behavior of the adder described in claims 1, 18, 33, 37, and 45 which *holds* the input values.

Therefore, the Smith reference teaches a system in which when the input changes, the output changes as well. Our system, in contrast, prevents output changes by *holding* the value of the inputs, and this technique provides the power savings that Smith does not offer or even suggest.

The First Office Action (on the first line of page 3) argued that the suppressor amounted to a transmission gate or latch:

> "The element (S, see figure 2d) can be seen as a transmission gate or latch with (a) as a logical input, (b) as clock input, and (c) as an output."

Applicants replied as follows:

First, that element S (called a SUPPRESSOR) in Smith's figure 2d shows that it is merely a two-input logic function whose output is described by a truth table. A transmission gate, by contrast, provides a high impedance between its input and its output when enabled. This provides the means of disconnecting an input when it is unwanted. No such function occurs in the Smith suppressor; it simply is *not* a transmission gate, nor is it a *latch*. Smith therefore does not disclose a circuit wherein any of its inputs are "held." The Smith suppressor does not disconnect input from output, let alone provide any *input-holding* feature; it merely provides a "logical zero" output signal value whenever enabled.

Second, it is incorrect to state that Smith's "second input (at 18)" is held by the "bypass input (K)," as is stated in the Office Action (on the fifth and sixth lines of item 4, on page 2), as the enabling signal for suppressor 18 is not associated with bypass input K.

The Final Office Action ignored Applicants' second point, and responded only to the first point:

> "In addition, the claims do not recite a limitation that requires the claimed "transmission gate" providing a high impedance output when enabled. Therefore, the element S in Smith that clearly disconnects its input (a) from its output (c) when enabled by control signal (b), or connects its input (a) to its output (c) when disabled by a control signal (b), can be seen as a transmission gate as claimed."

Applicants' answer is that the truth table for the suppressor itself contradicts this statement. The suppressor does not disconnect the input (a) from the output (c) when enabled by the control signal (b) ... instead, it sets the output to zero, which does not *hold* the input value ... it *passes* it half of the time (when the input is "N") and *changes* it half of the time (when the input is "Y").

Claim 18 recites a holding means, and is patentable for the same reason. Claim 18 further recites additional structure not disclosed in the Smith reference.

Likewise, claim 33 recites the step of holding at least one of the first and second inputs according to the bypass. Claim 33 is therefore also patentable over the Smith reference for the same reasons.

Claim 37 recites a second logic circuit element that conditionally holds one of the input values $A, B, \cdots$ according to the bypass input, as well as other structural features not described in the Smith reference. Claim 37 is therefore patentable on the same basis.

Claim 45 recites the step of conditionally holding one of the input values $A, B, \cdots$ according to the bypass input. Claim 45 is therefore patentable as well.

E. Claims 14 and 29 are Patentable Over the Smith Reference

Claim 14 recites:

> *A device for adding a signal at a first input (A) and a second input (B) to produce an adder output (S), comprising*
>
> *a bypass input (bypass); and*
>
> *a logic circuit, communicatively coupled to the bypass input (bypass), the first input (A), and the second input (B), the logic circuit configured to generate the adder output (S) without computing a new adder output according to the bypass input (bypass).*

The First Office Action indicated that inputs A and B correspond to Smith's E and P inputs, respectively.

Applicants disagreed, noting that Smith's suppressor 18 is not associated with bypass input K, and is not positioned to suppress input P. Smith, in fact, would not want to suppress the value of P, as Smith's purpose is that P should appear at the output T when the bypass K ("b" in the truth table of FIG. 2d) is on. Further, Smith's circuit is not configured to generate the adder output without computing a new adder output (Smith always computes a new adder output). The logic

used to compute the adder output *emulates* that the computations never took place, but the adder output is, in fact, computed anew nonetheless.

The Final Office Action responded that:

> "... it is respectfully submitted that the recitation "without computing a new adder output" does not require the adder not to compute a carry output. Therefore, the bypass [of] one of the arguments to the output of the adder as the sum without computing it in Smith clearly read[s] on this limitation."

In response, Applicants respectfully disagree that the phrase "without computing a new adder output" does not require the adder to not compute a carry output. Claims 14 and 29 recite "*a* new adder output" which includes a new adder output (S) or a new adder carry output (if there is a carry output). Further, Applicants note that dependent claim 17 specifically recites a carry output and that the carry output is regenerated without computing a new adder output.

Plainly, Smith does not teach a system that can generate the adder output without computing a new adder output (according to the bypass input). Whether the bypass signal is ON or OFF, the Smith system computes a new adder output. The new adder output may have the same *value* as the previous output, but a new adder output is computed just the same. In fact, Smith itself heralds this feature:

> Many prior art full binary adders and subtracters are known. However, none is known which has the capability of bypassing a function, while at the same time maintaining "circuit awareness" of the effect of not bypassing the function. Such a capability is particularly required in the high speed utilization of parallel computation techniques generally and, in certain aspects, serial computation techniques. This capability is especially important when the arithmetic unit is combined in an arithmetic complex (see the above copending application) which is to perform multiplication, division, power generation and root taking without non-pertinent peripheral computations.

Claim 29 recites features analogous to claim 14, and is patentable on the same basis.

F. Dependent Claims

Dependent claims 2-5, 9-10, 15-17, 19-22, 25, 26, 30-32, 34-36, 38-44, and 46-48 incorporate the features of their related independent claims, and are therefore patentable on this basis. In addition, these claims recite novel elements even more remote from the cited references. For example, with respect to claims 5, 10, 22, and 26, the Smith reference does not disclose a transmission gate adder, as described above.

VII. CONCLUSION

In view of the above, it is submitted that this application is now in good order for allowance and such allowance is respectfully solicited. Should the Examiner believe minor matters still remain that can be resolved in a telephone interview, the Examiner is urged to call Applicants' undersigned attorney.

Respectfully submitted,

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